MUNIAC

Munich Integrator And Computer

John G. Zabolitzky

Munich, Germany
Why build tube computer today?

- Difficult (close to impossible) to find original machine for collection (forget about working condition)
- Easier to maintain than original machine (e.g., parts availability)
- Achieve detailed understanding of historic machines, in particular design alternative decisions
Design Criteria

- Operate on standard German outlet, 230 V 16 A single phase = 4 kVA approx.
- word-parallel operation (not bit-serial)
- use existing magnetic core plane, found 4096 words of 12 bits (from DEC PDP-8)
- reasonable cost and effort
  - use available materials
  - performance of secondary importance
Gate-Level Design

- Need to devise logic module
- Want to have one single module type only
- dual miniature triodes for space/power
- single Eurocard => standard mechanics
- AND-OR-INVERT gate can do all
- use silicon diodes for logic, tubes for inverters (late 50s style)
Complex Logic

• Latch = two Gates
• Master-Slave Flip-Flop = two Latches = four Gates
• Multiplexers come for free (essentially)
• No Eccles-Jordan “Triggers” (Flip-Flops)
• Register = set of Master-Slave FFs
• Miniature Power Pentodes as clock drivers
Fig. 3
D
set clock
enable
clear clk
slave clock

master latch
slave latch
electron flow through the left tube. Applying negative shifts to the left side input point "A" will cause the right side input will flip a trigger such as this.

NOTE: Capacitive input triggers in the 604 respond only to negative shifts.

Figure 63. A Capacitive Input Trigger
Architecture

- Single accumulator, single address classical von Neumann machine (almost)
- "Very" von Neumann:
  - subroutining by code modification
  - indexing by code modification
    - overwrite addresses within code sequence
  - this is about 1950 style
Very Long Instruction Word (VLIW)

- 12 bit opcode, 12 bit operand/address
- only four basic operations:
  - operate (address)
  - operate (immediate)
  - jump conditional (cond, address)
  - store conditional (cond, address)
- operate fields: ALU, Carry, Datapath MUXes
Speed

- Latch pulse width: 3 \( \mu \)sec
- four non-overlapping clock phases
- \( \Rightarrow \) 16 \( \mu \)sec machine cycle time
  - 62.5 kHz
- 3 to 6 cycles per instruction
- \( \Rightarrow \) 10 KIPS = 0.01 MIPS
Effort and Calendar Time

- Inception: spring 1998
- design: summer 1998 (locate core plane)
- printed circuit board manufacture: fall 1998
- modules/card cages assembly: through 1999
- current: resting, logic about 1/2 completed
- core drive / sense largest missing part
- total est. 4000 hours, DM 20.000 parts